Subject: Re: Again ReadMemoryBarrier() etc
Posted by mirek on Mon, 09 Jul 2007 07:49:30 GMT
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Sorry, but this is the complete misunderstanding of the issue from several points of view.

First of all, these intrinsics are about COMPILER reordering! The do not emit any instructions, they just tell the compiler not to perform certain optimizations.

Second, they are not available on GCC and they behave differently on previous MSC versions.

Third, lfence / sfence are SSE instructions and believe or not, we still have to support CPUs without SSE.

Fourth, the idea that "the _WriteBarrier function forces writes to memory to complete at the point of the call. After the call, other threads can access the memory without fear that the thread that made the call might have a pending write to the memory." is wrong as well, even if you would thing that it emits actual CPU write barrier. This is not what a write barrier does for you... (but your mistake is quite understandable, because I was under this false impression too a couple of months ago....)

Mirek